CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (currently amended) A method for optimizing leakage power in a system comprising:

determining a static probability of a signal in the system; and

if the static probability is in a high power probability range, then modifying the signal such that the static probability of the modified signal is in a low power probability range, and such that functionality of the system is not affected;

wherein modifying the signal comprises modifying at least one of the group consisting of a source of the signal and a sink of the signal.

2. (original) The method of claim 1 wherein the signal is a digital signal, and modifying the signal comprises inverting the signal.

3. (currently amended) The method of claim 2 wherein the high power probability range is a probability range from 0 to 0.5.

4. (currently amended) The method of claim 2 wherein the high power probability range is a probability range from 0.5 to 1.

5. (original) The method of claim 2 wherein inverting the signal comprises inverting an output of a source of the signal and inverting an input of a sink of the signal.

6. (original) The method of claim 5 wherein inverting the output of the source comprises adding an inverter at the output of the source.

7. (original) The method of claim 5 wherein inverting the input of the sink comprises adding an inverter at the input of the sink.

8. (original) The method of claim 5 wherein the system comprises a programmable logic device, the programmable logic device comprising a lookup table, and wherein inverting the signal has no area or performance penalty.

9. (original) The method of claim 8 wherein inverting the output of the source comprises inverting each bit of the lookup table.

10. (original) The method of claim 8 wherein inverting the input of the sink comprises permuting the lookup table memory contents such that the lookup table expects an inverted input.

11. (currently amended) The method of claim 1 further comprising biasing the static probability by modifying the system such that the static probability is closer to the low power probability range.

12. (original) The method of claim 1 further comprising placing a source of the signal physically close to a sink of the signal.

13. (original) The method of claim 12 wherein the step of placing comprises assigning a high priority to the signal in a place and route operation.

14. (original) The method of claim 1 further comprising routing the signal in a manner that minimizes an objective function related to leakage power.

15. (original) The method of claim 14 wherein the objective function is based on leakage power consumed in circuits used to route the signal.

16. (currently amended) A machine readable storage having stored thereon a computer program having a plurality of code sections for optimizing leakage power in a system, the code sections executable by a machine for causing the machine to perform the steps of:

determining a static probability of a signal in the system; and

if the static probability is in a high power probability range, then modifying the signal such that the static probability of the modified signal is in a low power probability range, and such that functionality of the system is not affected;

wherein modifying the signal comprises modifying at least one of the group consisting of a source of the signal and a sink of the signal.

17. (original) The machine readable storage of claim 16 wherein the signal is a digital signal, and modifying the signal comprises inverting the signal.

18. (original) The machine readable storage of claim 17 wherein inverting the signal comprises inverting an output of a source of the signal and inverting an input of a sink of the signal.

19. (original) The machine readable storage of claim 18 wherein the system comprises a programmable logic device, the programmable logic device comprising a lookup table, and wherein inverting the signal has no area or performance penalty.

20. (original) The machine readable storage of claim 19 wherein inverting the output of the source comprises inverting each bit of the lookup table.

21. (original) The machine readable storage of claim 19 wherein inverting the input of the sink comprises permuting the lookup table memory contents such that the lookup table expects an inverted input.

22. (currently amended) A system optimized for reduced leakage power comprising:

a signal source having a modifiable output for sourcing a signal at the modifiable output; and

a signal sink having a modifiable input for sinking the signal at the modifiable input;

wherein the signal is selectively modified by the modifiable output and the modifiable input such that the signal has a static probability that is in a low power probability range, and such that functionality of the system is not affected.

23. (currently amended) The system of claim 22 wherein the signal is a digital signal, wherein the modifiable output is an invertible output, wherein the modifiable input is an invertible input, and wherein the signal is selectively inverted by the invertible output and the invertible input such that the signal has a static probability that is in the low power probability range, and such that functionality of the system is not affected.

24. (original) The system of claim 23 wherein the system comprises a programmable logic device having a lookup table, and wherein selectively inverting the signal has no area or performance penalty.

25. (original) The method of claim 24 wherein the signal source comprises a first lookup table, wherein the signal sink comprises a second lookup table, and wherein selectively inverting the signal comprises inverting each bit of the first lookup table and permuting the second lookup table memory contents such that the second lookup table expects an inverted input.